

\* TTL family :

- TTL Voltage / Current Rating

$A = 0$   
 $B = 0$  or each is 0  $\Rightarrow V_{out} = \text{high stat}$

$Q_3 \rightarrow \text{on}$   $Q_4 \rightarrow \text{off}$

Source current ( $I_{OH}$ )

$$= -400 \mu A$$

$A = 1$

$B = 1 \Rightarrow V_{out} = \text{Low stat (logic 0)}$

$Q_3 \rightarrow \text{off}$   $Q_4 \rightarrow \text{on}$

Sink current ( $I_{OL}$ )

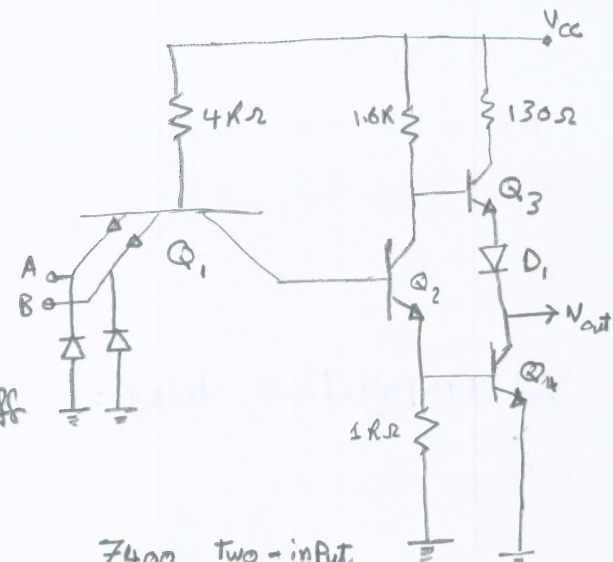
$$= 16 \text{ mA}$$

$$I_{ih} = 40 \mu A$$

$$I_{iL} = -1.6 \text{ mA}$$

$$\star \text{ Fan-out (Low-stat)} = \frac{|I_{OL}|}{|I_{iL}|} = \frac{16 \text{ mA}}{1.6 \text{ mA}} = 10 \text{ gates}$$

$$\star \text{ Fan-out (high-stat)} = \frac{|I_{OH}|}{|I_{ih}|} = \frac{400 \mu}{40 \mu} = 10 \text{ gates}$$



7400 Two-input  
NAND gate

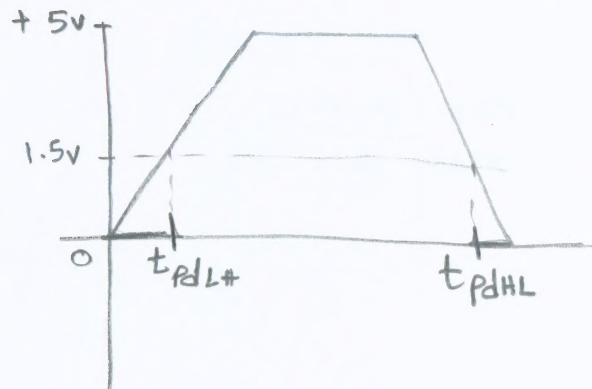
### \* Noise Margin

$$= 0.4 \text{ V}$$

up Low - stat voltage (0V: 0.8V)

down high stat voltage (2V: 5V)

### \* Propagation delay:



### \* Rise time $t_r$

Time of 10% : 90%  
of full voltage

$$0.5 \text{ V} : 4.5 \text{ V}$$

### \* Fall time $t_f$

time of 90% : 10% of full voltage

$$4.5 \text{ V} : 0.5 \text{ V}$$

### Power Dissipation:

$$P_D = V_{CC} * I_{CC}(\text{av})$$

$$I_{CC}(\text{av}) = \frac{I_{CCH} + I_{CCL}}{2}$$

